1. A method to produce an EEPROM for mass storage, comprising:

a) forming a plurality of polysilicon floating gates with a dielectric layer thereon upon an oxide layer on a semiconductor substrate above a plurality of wells implanted therein,

b) ion implanting a plurality of drain and plurality of source regions in said wells using said floating gates with sidewall spacers as a mask,

c) double diffusing said source regions with sidewall spacers adjacent to source region removed,

d) forming isolation oxidation, removing sidewall spacers adjacent to said drain regions and growing interpoly dielectric,

e) depositing a layer of polysilicon and forming a plurality of control gates over a plurality of said floating gates.

2. The method of claim 1 wherein, forming a thick floating gate provides a size of said sidewall spacer necessary to produce an offset for select transistor channel.

3. The method of claim 1 wherein, removing said sidewall spacers adjacent to said drain regions after said isolation oxidation retards oxidation on sides of said floating gates.

4. The method of claim 1 wherein, forming said plurality of control gates over a plurality of floating gates produces a plurality of word lines of a memory.

5. The method of claim 1 wherein, growing said interpoly oxidation provides a uniform field enhanced tunneling injector along edges of said floating gates to minimize endurance induced degradation caused by repeated erasing and reading of charge on said floating gate.

6. The method of claim 1 wherein, forming said floating gates with a thick dielectric is done to minimize floating gate to control gate coupling and allows a high field to be developed along edge of said floating gate during programming to permit fast charge transfer.

7. The method of claim 1 wherein, double diffusing said source regions and removing said sidewall spacers adjacent to source region is done with a shared masking step.

8. A non volatile memory, comprising:

a) flash memory cells organized in rows and columns,

b) cells in a row are interconnected by a wordline connecting to control gates of said flash memory cells in said row,

c) cell layout in a column mirrors cell layout in adjacent columns producing a first pair of adjacent columns with drains close together and a second pair of adjacent columns with sources close together,

d) a bit lines extend full length of said columns, laying between said first pair of adjacent columns and connecting said drains of said first pair of adjacent columns to a sense amplifier,

e) a source lines extend full length of said columns, laying between said second pair of adjacent columns and connecting said sources of said second pair of adjacent columns to source voltages.

9. The non volatile memory of claim 8 wherein, said wordlines are polysilicon lines laying over floating gates of said flash memory cells in said row and forming control gates for said flash memory cells.

10. The non volatile memory of claim 8 wherein, vertical page programming is done to cells in a selected column where the source line of said selected column is biased to a high positive voltage, the bit line of said selected column is biased to zero volts and the wordline of a selected cell in said selected column is biased to a positive voltage approximately equal to a threshold voltage of said flash memory cells with all other wordlines biased to zero volts and the bit line of said adjacent column of cells sharing said source line to a moderate positive voltage.

11. The non volatile memory of claim 8 wherein, horizontal page or block erase is done to cells in one or more rows of said non volatile memory by setting all bit lines, source lines and wordlines to zero volts, and applying a high positive voltage to the wordlines of the one or more rows to be erased.

12. The non volatile memory of claim 8 wherein, said memory cells are read by applying zero volts to the source line connected to a cell to be read, applying a positive voltage to the bit

line connected to the cell to be read, applying Vcc to the word line of the cell to be read, setting all other bit lines and source lines to said positive voltage, and setting all other wordlines to zero volts.

13. The non volatile memory of claim 8 wherein, cell layout in a column is a same cell layout in adjacent columns producing a first adjacent column with drains of cells connected to a first source line and sources of cells connected to a first bit line, and a second adjacent column with sources of cells connected to said first source line and drains of cells in said second adjacent column connected to a second bit line, allowing vertical page programming and horizontal page/block erase.

14. The non volatile memory of claim 13 wherein, bit lines extend full length of said columns, laying between a first pair of adjacent columns, connecting to said drains of a first column of said first pair of adjacent columns, to said sources of a second column of said first pair of adjacent columns, and connecting to a sense amplifier when performing a read operation.

15 The non volatile memory of claim 13 wherein, source lines extend full length of said columns, laying between a second pair of adjacent columns, connecting to said sources of a first column of said second pair of adjacent columns, connecting to said drains of said second pair of adjacent columns, and connecting to source voltages.

16. The non volatile memory of claim 8 wherein, cell layout in a column is an opposite cell layout in an adjacent column producing a first adjacent column with drains of cells connected to a first source line and sources of cells connected to a first bit line, and a second adjacent column with drains of cells connected to said first source line and sources of cell in said second adjacent column connected to a second bit line, allowing vertical page programming and horizontal page/block erase.

17. The non volatile memory of claim 16 wherein, bit lines extend full length of said columns, laying between a first pair of adjacent columns, connecting to said sources of a first column of said first pair of adjacent columns, to said sources of a second column of said first pair of adjacent columns, and connecting to a sense amplifier.

18 The non volatile memory of claim 16 wherein, source lines extend full length of said columns, laying between a second pair of adjacent columns, connecting to said drains of a first column of said second pair of adjacent columns, connecting to said drains of said second pair of adjacent columns, and connecting to a source voltage.

19. A method to produce an electrically erasable and programmable (EEPROM) for mass storage applications, comprising:

a) forming a well in a semiconductor substrate,

b) implanting ions into said well to establish a threshold voltage,

c) forming a gate isolation layer on top of said substrate,

d) forming a floating gate structure comprising a first layer of polysilicon with a dielectric insulator thereupon,

e) forming a sidewall spacer on sides of said floating gate structure,

f) ion implanting a plurality of drain and source regions in said well using said sidewall spacers as a mask,

g) removing sidewalls adjacent to said source regions,

h) double diffusing said source regions,

i) implanting a source within said source region,

j) depositing an isolation oxidation on source and drain regions and removing side wall spacers,

k) growing an interpoly dielectric,

l) depositing a second layer of polysilicon,

k) forming a control gate structure from said second layer of polysilicon and covering a plurality of said floating gate structures.

20. The method of claim 19 wherein, forming a thick floating gate structure provides a size of said sidewall spacer necessary to produce an offset for select transistor channel.

21. The method of claim 19 wherein, removing said sidewall spacers adjacent to said drain regions after said isolation oxidation retards oxidation on sides of said floating gates.

22. The method of claim 19 wherein, forming said plurality of control gates over a plurality of floating gates produces a plurality of word lines of a memory.

23. The method of claim 19 wherein, growing said interpoly oxidation provides a uniform field enhanced tunneling injector along edges of said floating gates to minimize endurance induced degradation caused by repeated erasing and reading of charge on said floating gate.

24. The method of claim 19 wherein, forming said floating gate structure with a thick dielectric is done to minimize floating gate to control gate coupling and allows a high field to be developed along edge of said floating gate during programming to permit fast charge transfer.

25. The method of claim 19 wherein, double diffusing said source regions and removing said sidewall spacers adjacent to source region is done with a shared masking step.